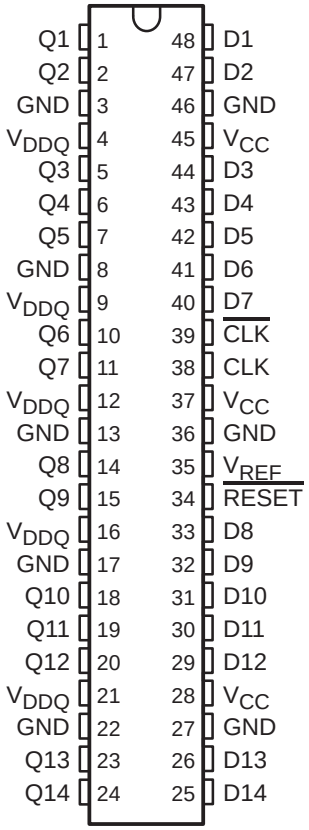
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports SSTL_2 Signal Data Inputs and Outputs**
- **Supports LVTTL Switching Levels on the $\overline{\text{RESET}}$ Pin**
- **Differential CLK Signal**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Meets SSTL_2 Class II Specifications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Packaged in Plastic Thin Shrink Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

This 14-bit registered buffer is designed for 2.3-V to 3.6-V V_{CC} operation and SSTL_2 data input and output levels.

All inputs are compatible with the JEDEC Standard for SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data and clock inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic high or low level.

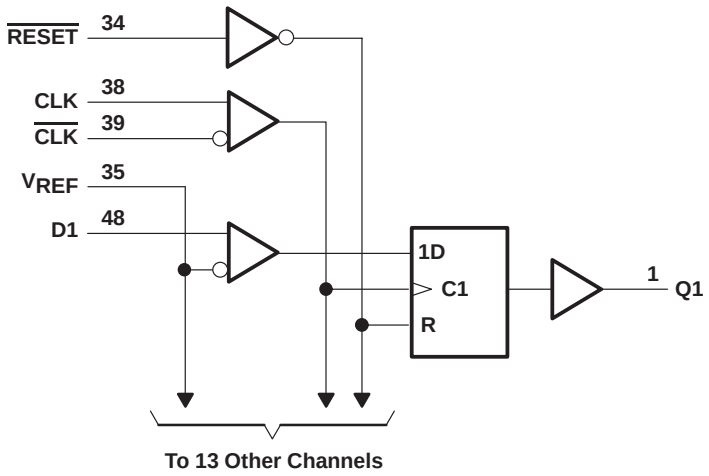
To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

The SN74SSTL16857 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUT
$\overline{\text{RESET}}$	$\overline{\text{CLK}}$	CLK	D	Q
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	L or H	X	Q_0

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . . ±50 mA
Continuous current through each V_{CC}, V_{DDQ}, or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 70°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. Current flows only when the output is in the high state and $V_O > V_{DDQ}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{DDQ}		3.6	V
V_{DDQ}	Output supply voltage		2.3		2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)		1.15	1.25	1.35	V
V_{TT}	Termination voltage		V_{REF}–40 mV	V_{REF}	V_{REF}+40 mV	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs	V_{REF}+350 mV			V
V_{IL}	AC low-level input voltage	Data inputs			V_{REF}–350 mV	V
V_{IH}	DC high-level input voltage	Data inputs	V_{REF}+180 mV			V
V_{IL}	DC low-level input voltage	Data inputs			V_{REF}–180 mV	V
V_{IH}	High-level input voltage	$\overline{\text{RESET}}$	2			V
V_{IL}	Low-level input voltage	$\overline{\text{RESET}}$			0.8	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{\text{CLK}}$	0.97		1.53	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{\text{CLK}}$	360			mV
I_{OH}	High-level output current				–20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{IK}		I_I = –18 mA		2.3 V			–1.2	V
V_{OH}		I_{OH} = –100 µA		2.3 V to 2.7 V	V_{CC}–0.2			V
		I_{OH} = –8 mA		2.3 V	1.95			
		I_{OH} = –16 mA			1.95			
V_{OL}		I_{OL} = 100 µA		2.3 V to 2.7 V			0.2	V
		I_{OL} = 8 mA		2.3 V			0.35	
		I_{OL} = 16 mA					0.35	
I_I	Data inputs	V_I = 1.7 V or 0.8V	V_{REF} = 1.15 V or 1.35 V	2.7 V			±5	µA
		V_I = 2.7 V or 0					±5	
		V_I = 1.7 V or 0.8V	V_{REF} = 1.15 V or 1.35 V	3.6 V			±5	
		V_I = 2.7 V or 0					±5	
	CLK, $\overline{CLK}$	V_I = 1.7 V or 0.8V	V_{REF} = 1.15 V or 1.35 V	2.7 V			±1	mA
		V_I = 2.7 V or 0					±1	
		V_I = 1.7 V or 0.8V	V_{REF} = 1.15 V or 1.35 V	3.6 V			±1	
		V_I = 2.7 V or 0					±1	
	$\overline{RESET}$	V_I = V_{CC} or GND		2.7 V			±5	µA
				3.6 V			±5	
	V_{REF}	V_{REF} = 1.15 V or 1.35 V		2.7 V			±5	
				3.6 V			±5	
I_{CC}		V_I = 1.7 V or 0.8 V	I_O = 0	2.7 V			90	mA
		V_I = 2.7 V or 0					90	
		V_I = 1.7 V or 0.8 V	I_O = 0	3.6 V			90	
		V_I = 2.7 V or 0					90	
C_i	$\overline{RESET}$	V_I = 1.7 V or 0.8 V		2.5 V†		3		pF
	Data inputs					2.5		
	$\overline{RESET}$	V_I = 1.7 V or 0.8 V		3.3 V‡		3		
	Data inputs					2.5		

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

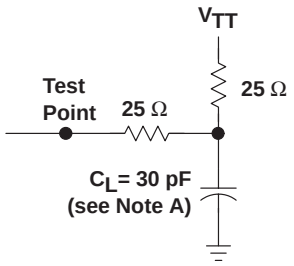
timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration, CLK, $\overline{CLK}$ high or low		3.3		3.3		ns
t_{su}	Setup time	Data before CLK↑, $\overline{CLK}$↓	1.1		1.75		ns
		$\overline{RESET}$ high before CLK↑, $\overline{CLK}$↓	0.6		1.1		
t_h	Hold time, data after CLK↑, $\overline{CLK}$↓		0.7		0.7		ns

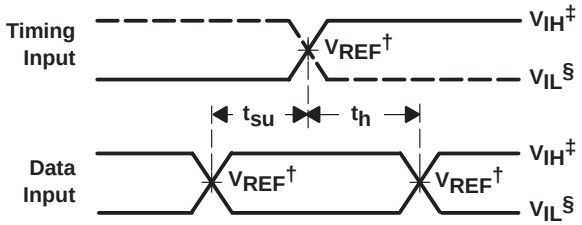
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{pd}	CLK and $\overline{CLK}$	Q	1.5	3.8	1.4	3.7	ns
t_{PHL}	$\overline{RESET}$	Q	1.5	4.3	1.4	3.5	ns

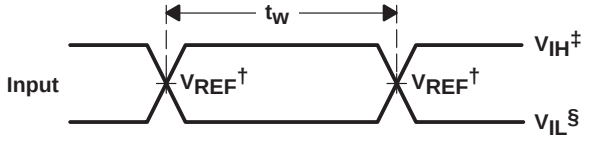
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V AND V_{CC} = 3.3 V ± 0.3 V



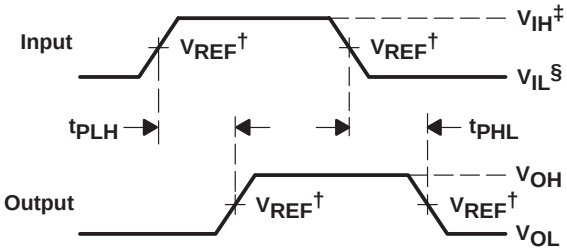
LOAD CIRCUIT



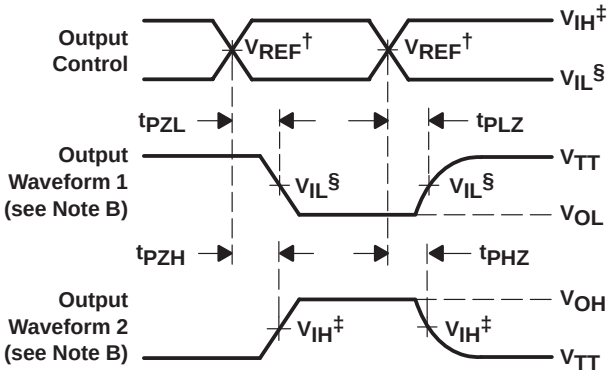
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

† $V_{REF} = V_{DDQ}/2$
‡ $V_{IH} = V_{REF} + 350$ mV (AC voltage levels)
§ $V_{IL} = V_{REF} – 350$ mV (AC voltage levels)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1.25 ns/V, t_f ≤ 1.25 ns/V.
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{TT} = V_{REF} = V_{DDQ}/2$
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74SSTL16857DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74SSTL16857DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74SSTL16857DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

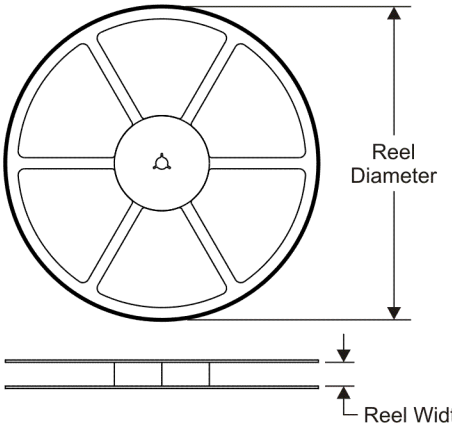
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

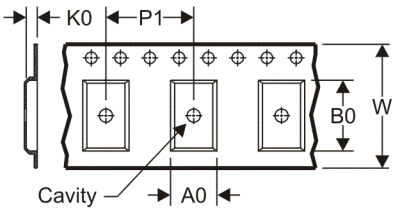
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

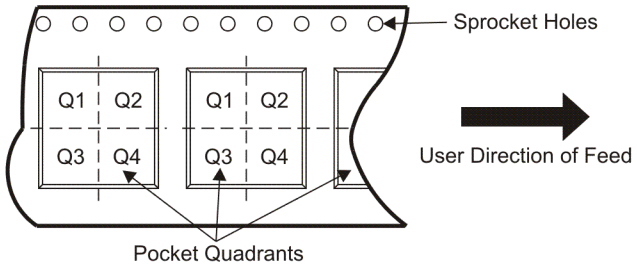


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

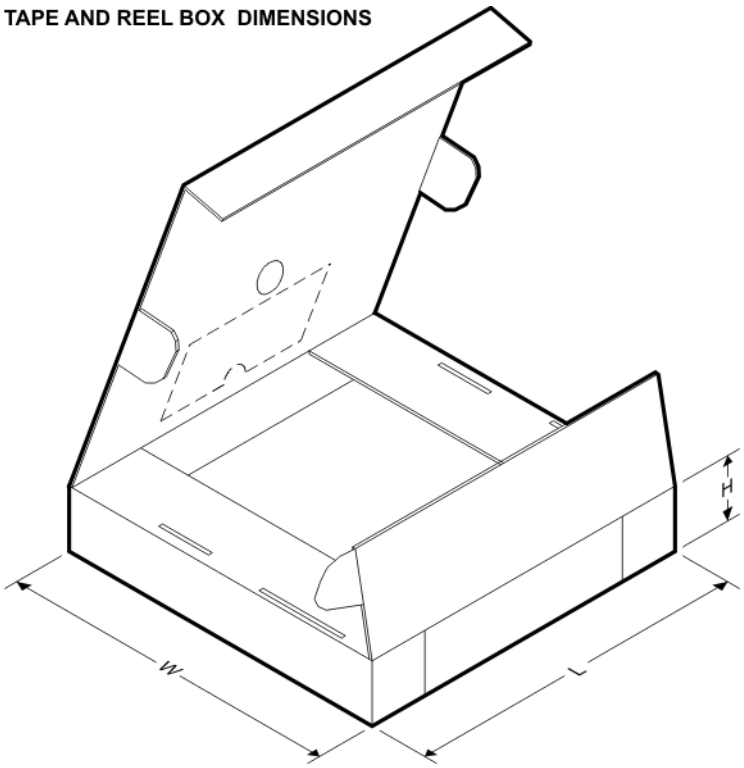
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTL16857DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

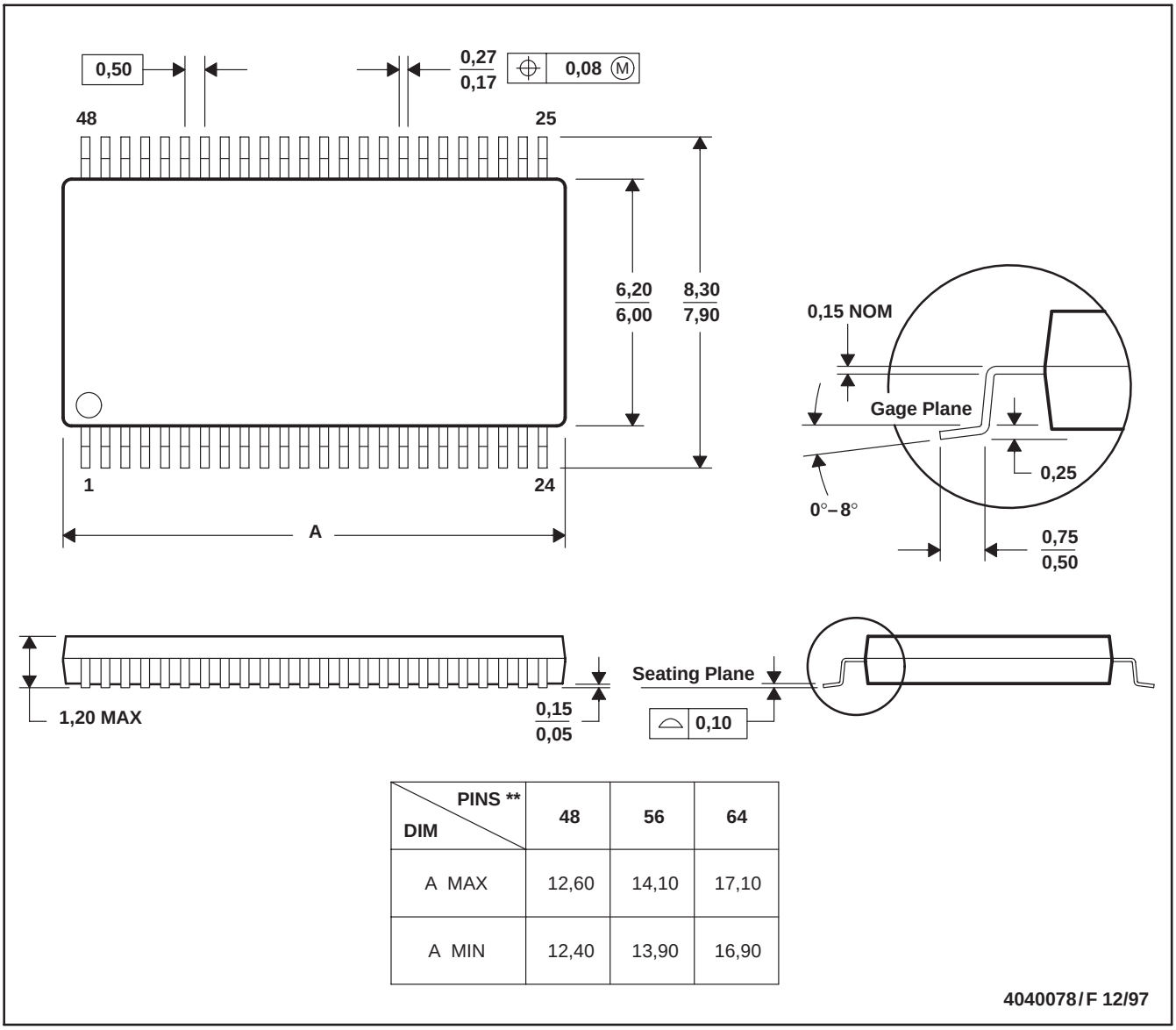


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTL16857DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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